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Design High Performance Combinational Circuits Using Output Prediction Logic-OPL Technique

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Abstract: *With the continuously increasing demand for low power & high speed VLSI circuits the brain storming among the scientists, inventors & researchers to find the techniques required to design such high performance circuits is also increasing day by day. In the answer to this search several design techniques have been found. Output prediction logic-OPL technique is one of such newly introduced techniques. OPL is a technique that can be applied to conventional CMOS logic families in order to obtain considerable speedups. Speedups of two to three times over static CMOS logic are demonstrated for a variety of combinational circuits. When applied to static CMOS the OPL retains the restoring nature of underlying logic family. In case of OPL applied to the pseudo NMOS & domino logic, the problem of excessive power dissipation is solved & speedups more than static CMOS logic is obtained.*

Keywords: *Output prediction logic-OPL technique, high speed & low power VLSI circuits, CMOS logic families.*

I. Introduction

Output prediction logic is a recently developed circuit technique that is twice as fast as domino logic and several times faster than conventional static CMOS logic. Output prediction logic is a technique that can be applied to different CMOS logic families to achieve considerable speedups. When applied to static CMOS, OPL retains the restoring character of the logic family. Dynamic circuit families such as domino are commonly used in today's high-performance microprocessors for obtaining timing goals that are not possible using static CMOS circuits [8,9]. Their increased performance is due to reduced input capacitance, lower switching thresholds, and circuit implementations that typically use fewer levels of logic due to the use of efficient and wide complex gates. It has been shown that dynamic logic can be used to realize average speed improvements of about 60% over static CMOS for random logic blocks when using synthesis tools tailored specifically for dynamic logic [9]. However, dynamic circuits have notable disadvantages. On-chip coupling noise in CMOS integrated circuits (ICs), until recently considered a second-order effect has become an important issue in deep sub-micrometer (DSM) CMOS integratedcircuits [10].In the case of domino, logic must be mapped to a unate network, which usually requires duplication of logic. Perhaps the main disadvantage going forward is its increased noise sensitivity (compared to static CMOS). The only way to increase its noise margin is to sacrifice some of its performance gain. How to retain the good attributes of static CMOS, namely high noise immunity and easy technology mapping, while obtaining greater speed is an elusive goal. Output prediction logic (OPL) is a new technique that can be applied to a variety of inverting logic families to increase speed while retaining the attributes of the underlying family. OPL relies on the alternating nature of logical output values for inverting gates on a critical path. That is, for any critical path, the logical output values of the gates along that path will be alternating ones and zeros. By correctly predicting exactly one half of the gate outputs, OPL obtains significant speedups (at least 2X) over the underlying logic families (e.g. Static CMOS, pseudo-nMOS and dynamic logic). When applied to static CMOS, OPL yields circuits that are typically 2 to 3 times faster than conventional static CMOS implementations. Although OPL employs clocks, OPL-static is inherently restoring logic and has the same noise margins as conventional static CMOS. OPL-static is also highly tolerant to clock skew, guaranteeing functionally correct results regardless of skew. Additionally, OPL-static uses the same synthesis tools as static CMOS. OPL can be applied to the same netlists as conventional static CMOS with a simple cell-for-cell substitution[8,9]. For the efficient implementation of wide NOR gates, designers often choose gates from pseudo-nMOS or dynamic logic families. OPL can be applied to these families as well to achieve higher speed performance. These speedups can be obtained while employing very conservative noise margins. In static CMOS logic, every gate is an inverting logic gate. Because of this inverting property, every output on a critical path must fully transition from 0 to 1, or 1 to 0 in the worst case. This is shown in figure 1, where we assume the primary input transitions high. This is why static CMOS is inherently slow. A circuit designer must take into account this worst-case delay scenario for a static CMOS critical path.

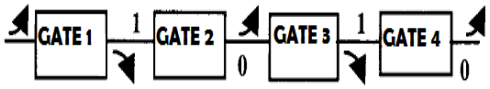

Figure 1: static CMOS worst case behavior [5]

Output prediction logic (OPL) greatly reduces the worst case behavior of critical path. OPL predicts that every inverting gate output on a critical path will be a logic one after the transitions are completed. Since all gates are inverting as in static CMOS the OPL predictions will be correct exactly the one half the time. Every other gate will not have to make transition. Every other gate will not have to make any transition as shown in figure 2.

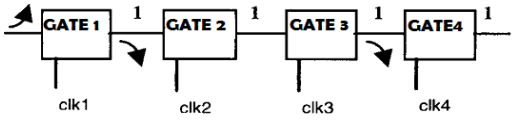

Figure 2: OPL predicting ones [5]

There is, however, a key problem with this idea. A one at every output (and therefore input) is not a stable state for an inverting gate. The one will erode (possibly going to zero) in the latter gates of a critical path.This can solved by tristating each gate with a clock. The timing specifications in clocking must be matched very carefully otherwise the glitches will corrupt the output or no impressive speedups can be achieved or the circuit will be clock blocked as in the case of CD logic. OPL is not a clock blocked technique that is the output is not controlled by the clocks involved but is data driven which requires careful clocking strategy. Here the successive clocks are delayed with an optimal delay. In work presented by McMurchie in 2000 and 2001 this delay was provided by using a reduced swing clock delay element which requires extra transistors and thus the area is also increased which is an undesirable factor in VLSI jargon. To find another technique to provide the required delay was needed that can be used to provide the necessary delay without increasing area drastically. This can be achieved by selecting proper transistor sizes. While an actual circuit essentially follows this desired behavior, there are important nonidealities. Figure 3 shows a chain of 3 OPL-static inverters.

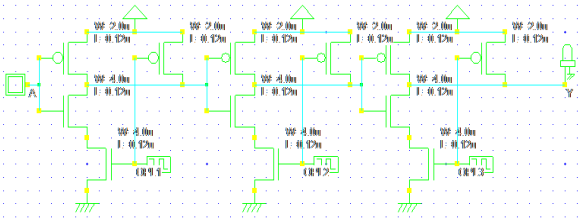

Figure 3: a chain of 3 OPL static inverters

II. Related work

A vast number of papers describing different circuit topologies and technologies have been reviewed in this work to attain the working knowledge of past as well as current trend in circuit designing. G. Divya et al. presented the power analysis of the full adder cells reported as having a low PDP (Power Delay Product), by means of speed, power consumption and area. These full adders were designed upon various logic styles to derive the sum and carry outputs. Two new high-speed and low-power full adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced PDP (Power-delay product). These all full adder cells designed using a TDK 90 nm CMOS technology [1].Sentamilselvi M. et al. described the designing of high performance adder circuit in VLSI system. The various parameters were considered for designing the circuit. The important parameters were power and delay. Different tools were used to perform the operation. However, the combinational circuit (i.e. adder) was designed by using different logic. The domino logic was the base of the proposed method. PMOS pull up network (PMOS PUN) was used to perform the operation. The proposed method included the tradeoff of the power and delay [2]. Chiranjeevi Pandamaneni et al. implemented low power high performance combinational circuits using output prediction logic. It was observed that output prediction logic (OPL) logic design style exhibit better characteristics (speed and power) as compared to other design styles. So, OPL logic style can be used where portability and high speed is the prime aim. Where, OPL consumes the lowest power among the three a technique that can be applied to conventional CMOS logic families obtained considerable speedups. Speedups of 2X to 3X over conventional static CMOS were demonstrated for a variety of circuits, ranging from chains of gates, to data path circuits, and to random logic

benchmarks [5].Sheng Sun et al. presented Output Prediction Logic, a technique that can be applied to conventional CMOS logic families to obtain considerable speedups. Average speedups of 2.35X over conventional static CMOS were demonstrated for a variety of circuits, ranging from chains of gates, to datapath circuits, and to random logic benchmarks. These speedups as obtained while retaining the noise margins and level restoring nature of static CMOS as well as the same netlists. OPL had excellent noise margins since each gate was a low-skew gate, quite unlike domino logic where critical paths consist of alternating low-skew and high- skew gates. They also designed a 64-bit. OPL-based adder that was more than twice as fast as the best previously reported adder [8].Larry McMurchie et al. presented Output Prediction Logic, a technique that can be applied to conventional CMOS logic families to obtain considerable speedups. Speedups of 2X to 3X over conventional static CMOS were demonstrated for a variety of circuits, ranging from chains of gates, to datapath circuits, and to random logic benchmarks. These speedups are obtained while retaining the noise margins and level restoring nature of static CMOS as well as the same netlists [9].

III. Mechanism

Each gate in all levels is tri-stated with a clock, in which case ones at inputs and a one output is no longer a contradiction for an inverting gate. The gates remain tristated until their inputs are ready for evaluation. In this manner, predicted output values are maintained until new input values dictate otherwise. Successive clocks are delayed by a clock separation as shown in figure 4.When the clock (clk) is low, the gate is tri-stated, with the output being charged to a logic one. When the clock goes high, the gate becomes a conventional static CMOS gate. there is an optimal point between the two extremes (fully clock-blocked and fully lost precharge values). The minimum delay occurs when a modest amount of glitch occurs. If the clock arrives at gate when its input is settling, a small glitch occurs. If the clock arrives earlier- when 50% point occurs at the same time as the 50% falling transition point then glitches will be enlarged. If the clock arrival is earlier yet then the precharged value is completely lost. The more effective approach is to use the following algorithm for optimized OPL:-

Algorithm {optimized_OPL}
For level 1 to number_of_levels (N)
    Run simulation for circuit
    For every gate in level (j)
        If a high gate output glitches below $V_{DD}/2$
        Double W_{effP} & W_{effN} (width_of_PMOS in PUN & NMOS in PDN)
    End for
    Run simulation for circuit
    For every gate in level
        If a high gate output glitches below $V_{DD}/2$
        Move gate clock ahead one phase
    End for
End for

A chain of four cascaded NOT gates designed using different logic families and OPL applied to them are shown in figure 5 as designed using static CMOS logic.

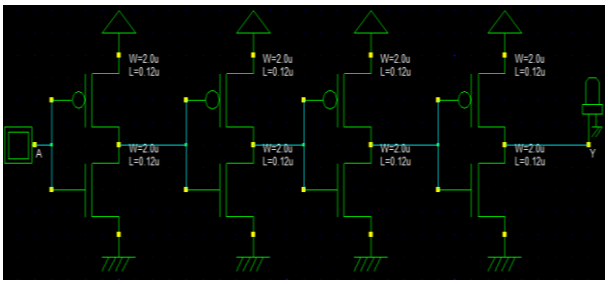

Figure 5: schematic of 4 NOT in static CMOS logic

Here, in the static CMOS logic,increasing levels of device integration, die size, and operating frequency, a burgeoning portable and embedded computing and communications market, combined with reliability and packaging cost concerns, have made power dissipation a major issue in VLSI design. In complementary static CMOS, a popular VLSI logic style,power is primarily dissipated during logic transitions when gate loadcapacitances charge and discharge[10]. Also the number of transistors required in static logic family is two times the number of inputs which increases the occupied area- an undesirable characteristic where

area limitations are in role. Still, many applications where area increment is not a constraint favor static CMOS logic due to it rail to rail operation. In such applications the delayand the power dissipation in static CMOS logic can be reduced by applying OPL technique as shown in figure 6.

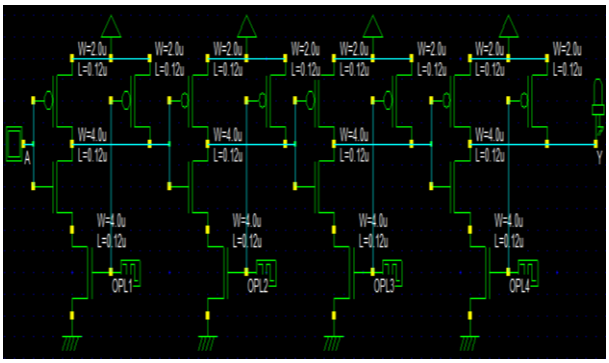

Figure 6: chain of 4 NOT using OPL static CMOS

Though the static CMOS logic offers less speed, it is best known for its lowest power dissipation [7]. As the number ofinputs increase, the number of transistors required will be doubled. In order to reduce the transistor count, pseudo NMOS is preferred, whereby area is also reduced. But itfails to improve speed and reduce power dissipation. Thenominal low output voltage for Pseudo NMOS is not 0V since, there is a fight between the devices in the pull down network and the grounded PMOS load device. This resultsin reduced noise margins and more importantly static power dissipation[3]**.** The chain of inverters designed in pseudo NMOS and domino logic are shown in figure 7&8.

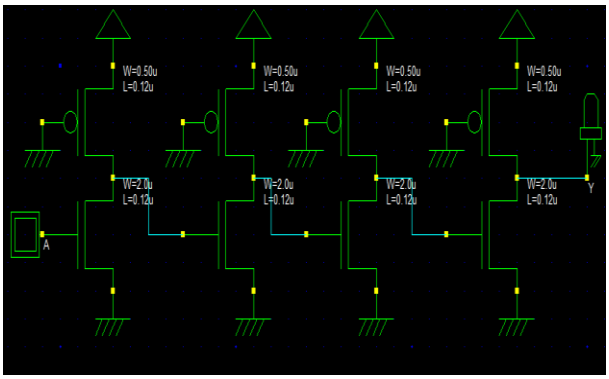

Figure 7: 4 NOT in pseudo NMOS LOGIC

The domino logic is a variation to the dynamic logic. Circuits designed using dynamic logic can not be cascaded directly due to the problem of monotonicity-a fundamental problem with dynamic circuits. While a dynamic gate is in evaluation the input can begin as a logical 0 & remain 0, begin 0 & remain 0, begin as 0 & rise to 0, begin as 1 and can remain 1 but it can notbegin as 1 & fall to 0 during evaluation. To solve this

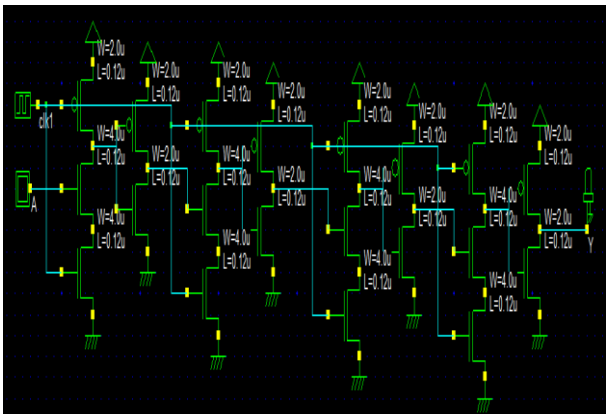

Figure 8: 4 NOT in domino logic

Problem an inverter is added to the output of every inverting gate which makes monotonically falling output into a monotonically falling signal suitable for next gate [6]**.** The power dissipation and delay are also a problem in dynamic/domino logic & pseudo NMOS logic which can be solved by applying OPL to these logic families as shown in figure 9& 10. Figure 9 shows 4 cascaded NOT in OPL pseudo NMOS & figure 10 shows 4 cascaded NOT in OPL domino logic.

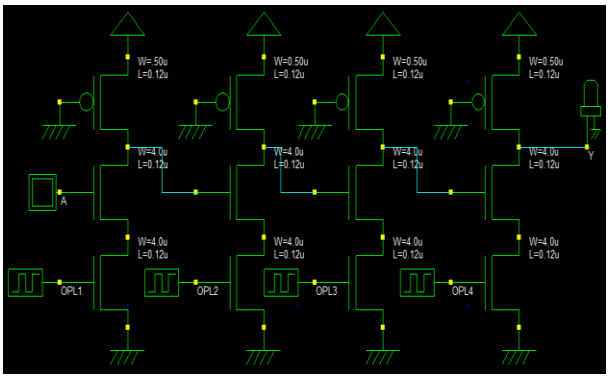

Figure 9: 4 cascaded NOT in OPL pseudo NMOS logic

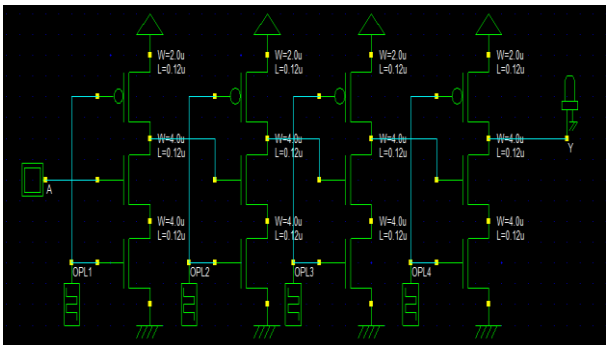

Figure 10: 4 NOT cascaded in OPL domino logic

IV. Results

Table 1 shows the comparison among different logic families for a chain of 4 inverters in terms of delay, powerdissipation, energy & surface area. Similar results have been obtained for a chain of four 3 input OR gates. The results for a chain of four 3 input OR gates is shown in table 2. The comparison among different logic families for a 2x1. It can be clearly seen that for a chain of 4 inverters designed using conventional CMOS logic the delay was reduced when OPL is applied. A speedup of 1.2 times for static is achieved for not chain. Similarly speed ups of 1.3x over pseudo NMOS & 9.1x over domino logic is achieved while working with 0.12µm technology, and supply voltage V_{DD} kept to be 1.2 volts.

Table 1: comparison among different logic families in terms of delay in nSec, power dissipation in mWatts, energy of output signal in mV and surface area, for a chain of four inverters.

Logic family	Delay in nSec.	Power dissipation in µW	Maximum energy in mV	Area in μm^2
Static CMOS	0.0390	0.033	319.97	167.9
OPL Static CMOS	0.0305	0.024	319.89	657.1
Pseudo NMOS	0.0355	0.586	308.80	127.8
OPL Pseudo NMOS	0.0260	0.515	308.68	571.5
Domino	0.0290	0.086	319.89	725.7
OPL Domino	0.0030	0.033	319.27	549.2

Also the power dissipation is reduced when OPL is applied to all the three conventional logic families. The chain of four 3 input OR gates and 2x1 multiplexer designed using different CMOS logic families and OPL applied to them also proved the extensively enhanced performance of the circuits employing output prediction logic OPL technique at the expense of some area increment for OPL application.

Table 2:comparison among different logic families in terms of delay in nSec,power dissipation in µWatts, energy of output signal in mV and surface area, for achain of four OR gates.

Logic family	Delay in nSec.	Power dissipation in µW	Maximum energy in mV	Area in μm^2
Static CMOS	0.0595	0.086	104.18mV	589.7
OPL Static CMOS	0.0105	0.015	118.74mV	1909.4
Pseudo NMOS	0.0625	1.021	102.21mV	464.7
OPL Pseudo NMOS	0.016	0.565	101.11mV	1131.4
Domino	0.0200	0.101	319.98mV	764.9
OPL Domino	0.0095	0.063	119.78mV	1441.6

Table 3: comparison of different logic families in terms of delay in nSec, power dissipation in mWatts, energy of output signal in mV and surface area for2x1 multiplexer

Logic family	Delay in nSec.	Power dissipation	Maximum energy in mV	Area in μm^2
Static CMOS	0.2615	0.086	246.85	179.6
OPL Static CMOS	0.0050	0.012	225.77	293.2
Pseudo NMOS	0.3295	0.265	224.94	111.2
OPL Pseudo NMOS	0.2855	0.147	226.52	506.6
Domino	0.0265	0.101	246.27	190.5
OPL Domino	0.0045	0.041	245.99	239.8

V. Conclusion

Output prediction logic OPL technique has been presented in this paper for a chain of four inverters, a chain of four 3 input OR gates and 2x1 multiplexer designed using static CMOS, pseudo NMOS and domino logic. Speedups of several times with a reduction in power dissipation were obtained when OPL is applied to the conventional CMOS logic families.

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